a third external terminal for receiving a write enable signal;

a fourth external terminal for receiving a signal which is used for designating one of said operational modes; and

control means for controlling the operation of access to a memory cell on the basis of said operational mode which is designated,

wherein said operational mode is designated in response to said column address strobe signal being at a logic "low" level, said write enable signal being at a logic "low" level and said signal being at a first predetermined logic level when said row address strobe signal is at a transitional logic level corresponding to a falling edge.

15. An address multiplex dynamic RAM according to claim 14, wherein said fourth external terminal is an address terminal.

~~16~~ 3. An address multiplex dynamic RAM according to claim ~~15~~ 2, wherein data is written ~~to a~~ into one of said memory ~~cell~~ cells on the basis of said operational mode.

~~17~~ 4. An address multiplex dynamic RAM according to claim ~~16~~ 3, wherein said one of said cells memory ~~cell~~ is designated on the basis of an address signal supplied to said fourth external terminal. ~~A~~

50